Journal of Mechanical Science and Technology 23 (2009) 1544~1552

Journal of Mechanical Science and Technology

www.springerlink.com/content/1738-494x DOI 10.1007/s12206-009-0108-y

# Optimization of rapid thermal processing for uniform temperature distribution on wafer surface<sup>†</sup>

Hyuck-Keun Oh<sup>1</sup>, Sae Byul Kang<sup>2</sup>, Young Ki Choi<sup>3</sup> and Joon Sik Lee<sup>1,\*</sup>

<sup>1</sup>Scholl of Mechanical & Aerospace Engineering, Seoul National University, Seoul, 151-742, Korea
 <sup>2</sup>Korea Institute of Energy Research, Daejeon 305-343, Korea
 <sup>3</sup>School of Mechanical Engineering, Chung Ang University, Seoul, 156-756, Korea

(Manuscript Received May 15, 2008; Revised September 25, 2008; Accepted January 13, 2009)

# Abstract

An optimization of rapid thermal processing (RTP) was conducted to obtain uniform temperature distribution on a wafer surface by using linear programming and radiative heat transfer modeling. The results show that two heating lamp zones are needed to maintain uniform wafer temperature and the optimal lamp positions are unique for a given geometry and not affected by wafer temperatures. The radii of heating lamps, which were obtained by optimization, are 45 mm and 108 mm. The emissivity and temperature of the chamber wall do not significantly affect the optimal condition. With obtained optimum geometry of the RTP chamber and lamp positions, the wafer surface temperatures were calculated. The uniformity allowance of the wafer surface is less than  $\pm 1$  °C when the mean temperature of the wafer surface is 1000 °C.

Keywords: Linear programming; Optimization; Rapid thermal processing; Uniform wafer temperature

## 1. Introduction

The semiconductor industry has prospered for the last 30 years, especially with dynamic random access memory (DRAM) and central processing unit (CPU). Many semiconductor fabrication companies have made efforts to develop new semiconductor fabrication techniques, even cutting down their profits in order to expand market share. There are many kinds of technical methods for reducing semiconductor manufacturing costs, such as shortening of the process time and increasing productivity. A furnace has been used as the heat treatment facility of semiconductor and has the advantage of heat treatment of a large number of wafers simultaneously, but has some defects, such as low productivity and relatively long process time. The rapid thermal processor (RTP) has replaced the furnace for RTP's capability of short process time. RTP is one of the semiconductor fabrication facilities of rapid wafer heating in several tens of seconds from room temperature to process temperature (600 ~ 1200 °C). RTP was developed in the late 1960's for manufacturing integrated circuits. It has many advantages such as high heating rate, clustered process in one RTP facility and so on. Many researches on the heat transfer phenomena of RTP have been conducted since late 1980's. These researches can be classified into two categories: developing an RTP model to predict the heat transfer characteristics and an optimizing control technique to obtain uniform temperature distribution on the wafer. In most of these researches, all RTP surfaces were considered as diffuse surfaces to simplify the problem.

There have been many studies for prediction and measurement of wafer temperature in various literatures. Kim et al. [1] constructed an RTP chamber with linear type tungsten-halogen lamps as a heating source and

<sup>&</sup>lt;sup>†</sup> This paper was recommended for publication in revised form by Associate Editor Dongsik Kim

<sup>\*</sup>Corresponding author. Tel.: +82 2 880 7117, Fax.: +82 2 883 0179 E-mail address: jslee123@snu.ac.kr

<sup>©</sup> KSME & Springer 2009

analyzed the capability of that system, which consists of ion implanting, annealing and oxidization process. Lord [2] predicted the wafer temperature and thermal stress by considering radiative and convective heat transfer, and compared the results with the experimental data. He concluded that convective heat transfer did affect wafer temperature uniformity in atmospheric pressure condition. Also, he suggested that the various shields could be helpful to prevent a temperature drop near the wafer edge. Campbell et al. [3, 4] presented the wafer temperature and gas flow pattern in RTP by numerical calculation and compared the results with the experimental data. They concluded that the radiative heat transfer by reflection had an insignificant effect on the heat transfer result of RTP and heat loss and that convective heat transfer must be considered to obtain uniform temperature distributions on the wafer surface. Norman [5, 6] conducted studies for wafer uniformity in steady state and transient state by multivariable control of heating lamps. There are few studies on finding the optimum positions and temperatures of heating lamps for uniform temperature distribution on the wafer surface. Jan and Lin [7] calculated the temperature of wafer for various heating lamp configurations. Their study was a kind of trial and error method; thus they found the optimum heating lamp configurations among many cases. Kim et al. [8] found the optimum powers of heating lamps to maintain uniform temperature distribution on the wafer by the optimization technique.

Many researches for uniform temperature on the wafer of RTP were conducted, such as numerical modeling, experimental study and control strategy of RTP. In the present study, an optimization procedure for uniform temperature on the wafer surface is developed through a well-known optimization technique, linear programming. We develop a 3-D radiative heat transfer calculation model for the RTP of diffuse surface through the above technique.

### 2. Radiative heat transfer model

In radiative heat transfer, surfaces can be classified as diffuse and specular. Diffuse surfaces reflect incident radiation into all direction regardless of the direction of incident radiation, and the reflected radiation is independent of reflection angle. Radiation is the dominant heat transfer mode in RTP, which occurs directly from the lamps to the wafer or one part on the wafer to another part on the wafer through reflection. The surfaces of the wafer and the chamber wall are assumed to be gray, diffuse [2, 6], opaque [9]. Radiative heat transfer can be easily calculated with view factor, irradiation, radiosity and assumptions such as gray surfaces whose emissivity and absorptivity are independent of wavelength of radiation spectrum, and diffuse surfaces. As this study focuses on the low-pressure rapid thermal processor (LPRTP), which has been investigated recently, convective heat transfer will not be considered.

A view factor  $F_{ij}$  is defined as the ratio of radiation leaving from surface *i* that is intercepted by surface *j* and can be obtained from the equation:

$$F_{ij} = \frac{1}{A_i} \int_{A_i} \int_{A_j} \frac{\cos \theta_i \cos \theta_j}{\pi R^2} dA_i dA_j$$
(1)

Eq. (1) is used to determine the view factor between two surfaces, those that are diffuse emitters and reflectors. On the basis of definition of the view factor, radiosity  $(J_i)$  and irradiation  $(G_i)$  of one surface can be defined. The energy balance can be applied at all surfaces. The heat transfer rate that leaves surface *i* is equal to the difference between the radiosity and irradiation and can be expressed as

$$q_i + G_i A_i - J_i A_i = 0 \tag{2}$$

The radiosity of the surface *i* consists of the emissive power and reflected irradiation of the surface and may be written as

$$J_i A_i = E_i A_i + \rho_i G_i A_i \tag{3}$$

The irradiation of the surface i can be calculated from the radiosities of all the surfaces in the enclosure and view factor:

$$G_{i}A_{i} = \sum_{j=1}^{N} F_{ji}J_{j}A_{j} = \sum_{j=1}^{N} F_{ij}J_{j}A_{i}$$
(4)

These entire variables can be expressed as a vector and matrix:

$$\mathbf{E} = \begin{bmatrix} E_1 & E_2 & \cdots & E_n \end{bmatrix}^T, \quad \mathbf{J} = \begin{bmatrix} J_1 & J_2 & \cdots & J_n \end{bmatrix}^T, \\ \mathbf{G} = \begin{bmatrix} G_1 & G_2 & \cdots & G_n \end{bmatrix}^T, \quad \mathbf{q} = \begin{bmatrix} q_1 & q_2 & \cdots & q_n \end{bmatrix}^T, \\ \boldsymbol{\varepsilon} = \begin{bmatrix} \varepsilon_1 & \varepsilon_2 & \cdots & \varepsilon_n \end{bmatrix}^T, \quad \mathbf{a} = \begin{bmatrix} A_1 & A_2 & \cdots & A_n \end{bmatrix}^T$$
(5)  
$$\mathbf{T}^4 = \begin{bmatrix} T_1^4 & T_2^4 & \cdots & T_n^4 \end{bmatrix}^T, \quad \mathbf{F} = \begin{bmatrix} F_{11} & F_{21} & \cdots & F_{n1} \\ F_{12} & F_{22} & \cdots & F_{n2} \\ \vdots & \vdots & \ddots & \vdots \\ F_{1n} & F_{2n} & \cdots & F_{nn} \end{bmatrix}$$

The heat transfer rate, radiosity and irradiation can be

rewritten by vector and matrix form by using Eq. (5):

$$\mathbf{q} = diag(\mathbf{a})\mathbf{J} - diag(\mathbf{a})\mathbf{G}$$
(6)

$$diag(\mathbf{a})\mathbf{J} = diag(\mathbf{a})\mathbf{E} + \mathbf{F}diag(\mathbf{a})\mathbf{J}$$
(7)  
$$diag(\mathbf{a})\mathbf{G} = \mathbf{F}diag(\mathbf{a})\mathbf{J}$$
(8)

From the above equations, the radiosity and irradiation can be substituted by the emissive power and view factor. Finally, the heat transfer rate of surface *i* can be expressed by the emissive power and view factor:

$$\mathbf{q} = (\mathbf{I} - \mathbf{F})(\mathbf{I} - (\mathbf{I} - diag(\mathbf{\epsilon}))\mathbf{F})^{-1}diag(\mathbf{a}\mathbf{\epsilon})\sigma\mathbf{T}^{4} \quad (9)$$

From Eq. (9), the heat transfer rate of all surfaces can be calculated in the case of gray-diffuse surfaces. Diffusive reflection surface is a reasonable assumption for most engineering situations and many studies also make the diffusive assumption as mentioned in the introduction.

The rapid thermal processor consists of heating lamps that convert electric energy into radiative heat energy, a wafer whose surface is to maintain uniform temperature, a quartz window that separates the heating lamps and wafer and the cold wall of the RTP chamber. Temperature of all parts of the RTP chamber except the cold wall is so high that the radiative heat transfer is the dominant heat transfer mechanism. The RTP chamber is cylindrical and the temperature of the cold wall is supposed to be 473 K (200°C). The lower face of the RTP consists of the wafer and wafer supporter that is the cold wall, and the side face of the RTP is the cold wall, and the upper zone of the RTP consists of the heating lamps. The grids for diffusive reflection surface of the RTP are generated. The view factor for a diffuse surface can be obtained by the well-established calculation method. The radiative heat transfer rate for diffuse surface can be calculated by employing the view factor, radiosity and irradiation.

## 3. Optimization procedure

The calculation domains are defined as follows: heating lamps, wafer and wall. For convenience, these terms are denoted by subscripts: L means the heating lamps, W the wafer and E the wall except the heating lamps and wafer. All domains are divided into grids and all the variables and constants are expressed in a vector form:

$$\mathbf{x} = [x_{E1} \cdots x_{El} \ x_{L1} \cdots \ x_{Lm} x_{W1} \cdots x_{Wn}]^T$$
(10)

Superscript T at Eq. (10) represents transpose operation of vector and  $\mathbf{x}$  means an arbitrary vector. From Eq. (10), there are n grids of wafer, m grids of heating lamps and l grids of wall.

There are many kinds of optimization methods. A proper optimization scheme can be chosen for each situation. Constraints for the present study are minimization of temperature difference of the wafer surface at steady state and heat balance of the RTP system, i.e., the 1<sup>st</sup> law of thermodynamics. Although the unsteady phenomenon is important characteristic in RTP, the system is considered steady. But the optimal location of heating lamps can be determined by steady optimization. If the locations of lamps are determined, the unsteady lamp power profile can be optimized by multivariable control [5]. So the scope of this study is confined to steady state.

The heating lamps cannot be heated over maximum temperature limit for their material property. Therefore, optimization for the present study is a minimization problem with three constraints. The radiative heat transfer rate for a diffuse surface can be calculated from the equation

$$\mathbf{q} = (\mathbf{I} - \mathbf{F})(\mathbf{I} - (\mathbf{I} - diag(\boldsymbol{\varepsilon}))\mathbf{F})^{-1}diag(\mathbf{a}\boldsymbol{\varepsilon})\sigma\mathbf{T}^{4}$$
  
=  $\mathbf{A} \cdot \mathbf{T}^{4}$  (11)

There is a linear relationship between the radiative heat transfer vector  $\mathbf{q}$  and the forth power of temperature  $\mathbf{T}^4$ . Because the objective function and constraints are linear type equations, the optimization problem for the present study can be easily resolved by linear programming. The objective function and constraints of linear programming are summarized as

$$\min_{\mathbf{x}} \mathbf{f}^{\mathsf{T}} \cdot \mathbf{x} \quad \text{such that} \\ \mathbf{A} \cdot \mathbf{x} \le \mathbf{b}, \ \mathbf{A}_{eq} \cdot \mathbf{x} = \mathbf{b}_{eq}, \ \mathbf{I} < \mathbf{x} < \mathbf{u}$$
(12)

The variables of the optimization problem for the present study are temperatures of heating lamps for uniform temperature distribution on the wafer surface. There are various methods to solve the optimization problem. From an engineering point of view, the optimization solution must be the minimum of energy supplied to heating lamps, i.e., the objective function of linear programming is minimizing the temperature of the heating lamp to maintain uniform temperature of the wafer surface. It can be represented as

$$\min_{T_L^4} \mathbf{f} \cdot \mathbf{T}_L^4 = \min \sum_{i}^{n_L} T_{L,i}^4$$
(13)

Where **f** is *ones*  $(1,n_L) = [1 \ 1 \ \cdots \ 1]$  and  $\mathbf{T}_L^4$  is  $[T_{L,1}^4 \ T_{L,2}^4 \ \cdots \ T_{L,n}^4]^T$ , meaning of heat flux vector emitted from the heating lamps. Eq. (13) represents that the objective function is finding minimum heat fluxes of heating lamps under some constraints. There are three constraints for the RTP system. The temperature of wafer surface must be within certain temperature bound at steady state and it can be expressed as

$$\mathbf{T}_{set} - \Delta \mathbf{T} < \mathbf{T}_{W} < \mathbf{T}_{set} + \Delta \mathbf{T}$$
(14)

But Eq. (14) is not an appropriate form as constraints. Eq. (11) can be expressed in terms of wafer, heating lamps and wall as

$$\mathbf{q} = [\mathbf{q}_{E}^{T} \ \mathbf{q}_{L}^{T} \ \mathbf{q}_{W}^{T}]^{T} = \mathbf{A} \cdot \mathbf{T}^{4}$$
$$= \begin{bmatrix} \mathbf{A}_{E,E} & \mathbf{A}_{E,L} & \mathbf{A}_{E,W} \\ \mathbf{A}_{L,E} & \mathbf{A}_{L,L} & \mathbf{A}_{L,W} \\ \mathbf{A}_{W,E} & \mathbf{A}_{W,L} & \mathbf{A}_{W,W} \end{bmatrix} \cdot \begin{bmatrix} \mathbf{T}_{E}^{4} \\ \mathbf{T}_{L}^{4} \\ \mathbf{T}_{W}^{4} \end{bmatrix}$$
(15)

It is easy to extract the heat transfer rate for wafer surface from the above equation.

$$\mathbf{q}_{\mathrm{W}} = \mathbf{A}_{\mathrm{W},\mathrm{E}} \cdot \mathbf{T}_{\mathrm{E}}^{4} + \mathbf{A}_{\mathrm{W},\mathrm{L}} \cdot \mathbf{T}_{\mathrm{L}}^{4} + \mathbf{A}_{\mathrm{W},\mathrm{W}} \cdot \mathbf{T}_{\mathrm{W}}^{4}$$
(16)

where  $T_W^4$  and  $T_E^4$  are constant vectors which represent fourth power of wafer and wall temperature at steady state, respectively. Matrix **A** is determined by the view factor and radiative properties. The heat transfer rate of wafer,  $\mathbf{q}_W$  becomes **0** at steady state. Therefore, Eq. (16) becomes

$$\mathbf{A}_{\mathrm{W,E}} \cdot \mathbf{T}_{\mathrm{E}}^{4} + \mathbf{A}_{\mathrm{W,L}} \cdot \mathbf{T}_{\mathrm{L}}^{4} + \mathbf{A}_{\mathrm{W,W}} \cdot \mathbf{T}_{\mathrm{W}}^{4} = \mathbf{0}$$
(17)

If the temperature of the wafer  $\mathbf{T}_{W}$  is  $\mathbf{T}_{set} - \Delta T$ or  $\mathbf{T}_{set} + \Delta T$ , then Eq. (17) becomes

$$\mathbf{A}_{\mathrm{W,E}} \cdot \mathbf{T}_{\mathrm{E}}^{4} + \mathbf{A}_{\mathrm{W,L}} \cdot \mathbf{T}_{\mathrm{L}}^{4} + \mathbf{A}_{\mathrm{W,W}} \cdot (\mathbf{T}_{set} - \Delta \mathrm{T})^{4} < \mathbf{0} \ (18)$$

$$\mathbf{A}_{\mathrm{W,E}} \cdot \mathbf{T}_{\mathrm{E}}^{4} + \mathbf{A}_{\mathrm{W,L}} \cdot \mathbf{T}_{\mathrm{L}}^{4} + \mathbf{A}_{\mathrm{W,W}} \cdot (\mathbf{T}_{set} + \Delta T)^{4} > \mathbf{0} (19)$$

If the temperature of the wafer is less than the temperature of steady state condition, i.e.,  $\mathbf{T}_{W} = \mathbf{T}_{set} - \Delta T$ , the net radiation is absorbed into the wafer surface, i.e., the heat flux becomes negative. On the other hand, if the temperature of the wafer is larger than the temperature of steady state, i.e.,  $\mathbf{T}_{W} = \mathbf{T}_{set} + \Delta T$ , then the net radiation leaves wafer surface, and the heat flux becomes positive. Thus, the

Table 1. Definitions of the objective function and constraints in the linear programming.

Linear programming	Present Study
$\min_{\mathbf{X}} \mathbf{f}^{T} \cdot \mathbf{x}$	$\mathbf{f} = ones(n_L, 1) = \begin{bmatrix} 1 & 1 & \cdots & 1 \end{bmatrix}^{\mathrm{T}}$
	$\mathbf{x} = \mathbf{I}_{\mathrm{L}}$
$\mathbf{A} \cdot \mathbf{x} \leq \mathbf{b}$	$\mathbf{A} = \begin{bmatrix} \mathbf{A}_{\mathrm{W,L}} \\ -\mathbf{A}_{\mathrm{W,L}} \end{bmatrix}$
	$\mathbf{b} = \begin{bmatrix} -\mathbf{A}_{\mathrm{W},\mathrm{E}} & -\mathbf{A}_{\mathrm{W},\mathrm{W}} & 0 \\ \mathbf{A}_{\mathrm{W},\mathrm{E}} & 0 & \mathbf{A}_{\mathrm{W},\mathrm{W}} \end{bmatrix} \cdot \begin{bmatrix} \mathbf{T}_{\mathrm{E}}^{4} \\ (\mathbf{T}_{\mathrm{set}} - \Delta \mathbf{T})^{4} \\ (\mathbf{T}_{\mathrm{set}} + \Delta \mathbf{T})^{4} \end{bmatrix}$
$\mathbf{A}_{eq} \cdot \mathbf{x} = \mathbf{b}_{eq}$	$\mathbf{A}_{eq} = (\mathbf{A}_{E,L} + \mathbf{A}_{L,L})$
	$\mathbf{b}_{eq} = -[\mathbf{A}_{E,E} + \mathbf{A}_{L,E} \ \mathbf{A}_{E,W} + \mathbf{A}_{L,W}] \cdot \begin{bmatrix} \mathbf{T}_{E}^{4} \\ \mathbf{T}_{W}^{4} \end{bmatrix}$
I < x < u	$\mathbf{I} = \mathbf{T}_{\min}^4$
	$\mathbf{u} = \mathbf{T}_{\max}^4$

fourth power of temperature of heating lamps can be expressed as an inequality form from Eqs. (18) and (19).

$$\begin{bmatrix} \mathbf{A}_{\mathrm{W},\mathrm{L}} \\ -\mathbf{A}_{\mathrm{W},\mathrm{L}} \end{bmatrix} \cdot \mathbf{T}_{\mathrm{L}}^{4}$$

$$< \begin{bmatrix} -\mathbf{A}_{\mathrm{W},\mathrm{E}} & -\mathbf{A}_{\mathrm{W},\mathrm{W}} & \mathbf{0} \\ \mathbf{A}_{\mathrm{W},\mathrm{E}} & \mathbf{0} & \mathbf{A}_{\mathrm{W},\mathrm{W}} \end{bmatrix} \cdot \begin{bmatrix} \mathbf{T}_{\mathrm{E}}^{4} \\ (\mathbf{T}_{set} - \Delta \mathbf{T})^{4} \\ (\mathbf{T}_{set} + \Delta \mathbf{T})^{4} \end{bmatrix}$$
(20)

The RTP system must satisfy the heat balance condition at steady state. Thus the summation of the heat transfer rate of wafer, lamps and walls becomes zero.

$$\mathbf{q}_{\mathrm{E}} + \mathbf{q}_{\mathrm{L}} + \mathbf{q}_{\mathrm{W}} = \mathbf{q}_{\mathrm{E}} + \mathbf{q}_{\mathrm{L}} = \mathbf{0}$$
(21)

$$\begin{bmatrix} \mathbf{A}_{\mathrm{E},\mathrm{E}} & \mathbf{A}_{\mathrm{E},\mathrm{L}} & \mathbf{A}_{\mathrm{E},\mathrm{W}} \end{bmatrix} \cdot \begin{bmatrix} \mathbf{T}_{\mathrm{E}}^{4} \\ \mathbf{T}_{\mathrm{L}}^{4} \\ \mathbf{T}_{\mathrm{W}}^{4} \end{bmatrix}$$
(22)

$$+\begin{bmatrix} \mathbf{A}_{\mathrm{L,E}} & \mathbf{A}_{\mathrm{L,L}} & \mathbf{A}_{\mathrm{L,W}} \end{bmatrix} \cdot \begin{bmatrix} \mathbf{T}_{\mathrm{E}}^{4} \\ \mathbf{T}_{\mathrm{L}}^{4} \\ \mathbf{T}_{\mathrm{W}}^{4} \end{bmatrix} = \mathbf{0}$$
$$(\mathbf{A}_{\mathrm{E,L}} + \mathbf{A}_{\mathrm{L,L}})\mathbf{T}_{\mathrm{L}}^{4} =$$
$$-\begin{bmatrix} \mathbf{A}_{\mathrm{E,E}} + \mathbf{A}_{\mathrm{L,E}} & \mathbf{A}_{\mathrm{E,W}} + \mathbf{A}_{\mathrm{L,W}} \end{bmatrix} \cdot \begin{bmatrix} \mathbf{T}_{\mathrm{E}}^{4} \\ \mathbf{T}_{\mathrm{W}}^{4} \end{bmatrix}$$
(23)

Eqs. (21), (22) and (23) represent the same meaning that is the heat balance of the RTP system. The



Fig. 1. Schematic of an RTP chamber with dimensions (unit: mm).



Fig. 2. The lamp temperature distribution at a steady state wafer temperature of 873 K when  $T_E = 473$  K and  $\varepsilon_E = 0.2$ .

last constraint is the temperature range of the heating lamp. The filament of the heating lamp, tungstenhalogen lamp, is made of tungsten. Thus, it is impossible to heat the tungsten-halogen lamp over a certain temperature. This constraint is expressed in terms of the maximum and minimum temperature as

$$\mathbf{T}_{\min} < \mathbf{T}_{L} < \mathbf{T}_{\max} \tag{24}$$

The objective function and constraints for the present study are compared with the canonical form of linear programming in Table 1. Linear programming is a well-known optimization technique and can be easily programmable by MATLAB<sup>®</sup> (The Math Works Inc., version 5.3).

#### 4. Optimization results

All the surfaces in the RTP system are idealized as diffuse surfaces to calculate the view factor. The shape and dimension of the RTP system are shown in Fig. 1. Although a 300 mm (12 inch) wafer is the most common size, the system for the 200 mm (8 inch) wafer is considered in this paper to simplify optimization. But this study focuses on the optimization procedure, which will be the same without reference to wafer size. The wall of the RTP chamber is assumed to be the boundary conditions of constant temperature and emissivity.

The grids of heating lamps at the top wall of the RTP system are generated along the radial direction. The number of grids is 50 and the grid interval is constant along the radial direction to determine optimal lamp position accurately. The grids at the wafer are different from those of heating lamps. Each grid at the wafer is generated in the manner that all of the areas of grid at the wafer are same. The number of grids for the wafer surface is also 50.

To calculate the radiative heat transfer rate for a diffuse surface, the entire view factor of the RTP chamber must be determined. To check the correctness of the view factor calculation, it is confirmed that summation of the view factor from one grid to the other grids becomes 1 from the equation

$$\sum_{i} F_{ij} = 1 \quad \text{for all } i \tag{25}$$

The walls in the RTP chamber except heating lamps and wafer are treated as the boundary condition of constant temperature and emissivity. Optimization is conducted when the temperature and emissivity of the wall is 200  $^{\circ}$ C and 0.20, respectively. Figs. 2 and 3 show the optimum temperature distributions of heating lamps to obtain a uniform wafer temperature of 873 and 1273 K at steady state (uniform wafer temperature does not mean exactly uniform temperature but temperature with small difference). The minimum temperature of heating lamps is 473 K and the heating lamps are assumed as diffuse-gray surface of  $\varepsilon = 0.8$ . Fig. 2 shows the optimum temperature distribution of the heating lamps to make the wafer temperature uniform at 873 K. Despite the fact that all the top surfaces of the RTP chamber are assumed to be heating lamps, only two zones of heating lamps are required to keep the wafer temperature 873 K and the other zones of heating lamps maintain the minimum temperature 473 K. The radii of two zones of high temperature are 42  $\sim$  48 mm, 105  $\sim$  111 mm as one can see in Fig. 2. This trend also appears at the other case in Fig. 3 ( $T_w$ =1273 K). Figure 4 shows the optimum temperature distributions of the heating lamps for various wafer temperatures in the same graph. The positions of the heating lamps are identical for all cases, as seen in Fig. 4. As the wafer temperature increases, the temperature of the heating lamps also increases. Fig. 5 shows the schematic diagram of the heating lamps. In Fig. 5, the circle of dashed line



Fig. 3. The lamp temperature distribution at a steady state wafer temperature of 1273 K when  $T_E = 473$  K and  $\varepsilon_E = 0.2$ .



Fig. 4. The lamp temperature distribution for various wafer temperatures at  $T_E = 473$  K and  $\varepsilon_E = 0.2$ .



Fig. 5. The optimum lamp position ( --- : wafer,  $\blacksquare$  : heating lamps).

represents 200 mm wafer, and two zones of gray coaxial annular represent heating lamps based on the optimization results. In brief, the positions of the heating lamps are constant regardless of wafer temperature for the given shape of the RTP chamber. The



Fig. 6. The wafer temperature distribution for  $T_{ser} = 873$  K at the optimum condition of the heating lamp.



Fig. 7. The wafer temperature distribution for  $T_{set} = 1273$  K at the optimum condition of the heating lamp.



Fig. 8. The wafer temperature distributions for various wafer temperatures at the optimum condition of the heating lamps.

wafer temperature can be obtained by optimization. From Eq. (17), the optimum temperatures of the lamp  $T_L^4$  are obtained by optimization.

Thus the wafer temperatures  $T_{\rm W}^4$  , can be determined from the equation

$$\mathbf{T}_{W}^{4} = \mathbf{A}_{W,W}^{-1} \cdot (\mathbf{A}_{W,E} \cdot \mathbf{T}_{E}^{4} + \mathbf{A}_{W,L} \cdot \mathbf{T}_{L}^{4})$$
(26)

Figs. 6 and 7 show the wafer temperature distributions at optimum condition for  $T_{set} = 873$  K and 1273 K.



Fig. 9. The maximum wafer temperature differences at various steady state temperature at  $T_E = 473$  K,  $\varepsilon_E = 0.2$ .



Fig. 10. The lamp temperature distributions for various wafer temperatures at  $T_E = 373$  K,  $\varepsilon_E = 0.2$ .

Maximum temperature differences on the wafer surface are small for both cases. Figure 8 shows the temperature differences on the wafer surface for each case at steady state. The temperature difference is about 1.1 K at  $T_w = 673$  K and 4.6 K at  $T_w = 1473$  K. Fig. 9 shows the temperature difference on the wafer surface for each case at steady state. To check the effects of a wall temperature on optimization results, optimization is performed at  $T_E = 373$  K, and  $\varepsilon_E =$ 0.20. The other properties are identical to those of the previous calculation. However, the minimum temperature of the heating lamps is 373 K, which is the same as the temperature of the wall. The temperature of the heating lamps by optimization can be seen in Fig. 10. From the figure, the optimum positions of the heating lamps at  $T_E = 373$  K are identical to the optimum results for  $T_E = 473$  K.

Effects of wall emissivity on optimization results are also studied. Optimizations are conducted with the values  $\varepsilon_E = 0.18$  and 0.22. The wall temperature in this case is 373 K. The optimum positions of the heating lamps for  $\varepsilon_E = 0.18$  (Fig. 11) and 0.22 (Fig. 12) are at 42 ~ 48 mm, 105 ~ 111 mm. Same trends go for  $\varepsilon_E = 0.20$  (Fig. 10). It is evident that a small



Fig. 11. The lamp temperature distributions for various wafer temperatures at  $T_E = 373$  K,  $\varepsilon_E = 0.18$ .



Fig. 12. The lamp temperature distributions for various wafer temperatures at  $T_E = 373$  K,  $\epsilon_E = 0.22$ .

change in wafer emissivity does not affect optimization results.

#### 5. Conclusions

An optimization scheme, linear programming, is used to obtain uniform temperature distributions on the wafer surface for rapid thermal processing. A gray-diffuse surface assumption is adopted to calculate radiative heat transfer rate. The temperature distributions on the wafer are calculated by optimization.

Some important aspects of the present study can be summarized as follows.

An optimization procedure for rapid thermal processing is presented in detail. The objective function is minimized for the powers of heating lamps and the constraints are heat balance of the RTP chamber, temperature bounds of the wafer at steady state and temperature limits of the heating lamps. From the result of optimization, two zones of heating lamps are needed to obtain uniform temperature of the wafer. The optimal lamp positions are unique for a given geometry and not affected by wafer temperatures. The radii of heating lamps, which are obtained by optimization, are 42 ~48 mm and  $105 \sim 111$  mm. The emissivity and temperature of the chamber wall do not significantly affect the optimal condition. The wafer surface temperatures are calculated by optimization. The temperature difference of the wafer surface is about ±2 K when the mean temperature of the wafer surface is 1273 K.

## Acknowledgment

This work was supported by the Micro Thermal System Research Center, Seoul National University, sponsored by the Korean Science and Engineering Foundations, and by the Korea Research Foundation Grant (KRF-J03002).

#### References

- Y. T. Kim, K. R. Jung, H. Y. Kim, H. T. Kim and H. J. Yoo, Development and application of rapid thermal processing, *Journal of KIEE (*in Korean) 10 (9) (1988) 1051-1058.
- [2] H. A. Lord, Thermal and stress analysis of semiconductor wafers in a rapid thermal processing oven, *IEEE Transactions on Semiconductor Manufacturing*, 11 (3) (1988) 105-114.
- [3] S. A. Campbell, K. L. Knutson, K. H. Ahn, J. D. Leighton and B. Y. H. Liu, Gas flow patterns and thermal uniformity in rapid thermal processing equipment, *International Electron Devices Meeting*, (1990) 921-924.
- [4] S. A. Campbell, K. H. Ahn, K. L. Knutson, B. Y. H. Liu and J. D. Leighton, Steady-state thermal uniformity and gas flow patterns in a rapid thermal processing chamber, *IEEE Transactions on Semiconductor Manufacturing*, 4 (1) (1992) 14-20.
- [5] S. A. Norman, Optimization of transient temperature uniformity in RTP Systems, *IEEE Transactions* on Electron Devices, 39 (1) (1992) 205-207.
- [6] S. A. Norman, Wafer temperature control in rapid thermal processing, PH.D. Thesis, Stanford Univ., Stanford, California, (1992).
- [7] Y. K. Jan and C. A. Lin, Lamp configuration design for rapid thermal processing systems, *IEEE Transactions on Semiconductor Manufacturing*, 11 (1) (1988) 75-84.
- [8] S. J. Kim, S. B. Kang, S. Y. Hyun, Y. M. Cho, J. D. Chung, J. S. Lee, C. H. Jung, Y. J. Choi and K. R. Jung, Performance analysis of a rapid thermal processor via physics-based modeling and convex op-

timization, *IEEE International Symposium on Industrial Electronics*, (2001) 1213-1218.

[9] F. Y. Sorrel, M. J. Fordham, M. C. Ozturk and J. J. Wortman, Temperature uniformity in RTP furnaces, *IEEE Trans. Electron Device*, 39 (1) (1992) 75.



Hyuck-Keun Oh received the B.S. and M.S degrees in Mechanical & Aerospace Engineering from Seoul National University in 2000 and 2002, respectively. He had experienced mechanical and electrical

engineering in the Samsung SDI Corporation on various display devices between 2002 and 2007. He is now pursuing the Ph.D degree in Mechanical & Aerospace engineering at Seoul National University, Korea. His research interests are heat transfer and thermal management with a focus on power generation and energy efficiency.



Sae Byul Kang received the B.S degree in Mechanical engineering from Korea University in 1996. He then went on to receive his M.S and Ph.D. degrees from Seoul National University in 1998 and 2003, respectively. Dr. Kang is

currently a senior researcher at the Korea Institute of Energy Research in Daejeon, Korea. Dr. Kang's research interests are development of industrial boiler and burner for bio-mass.



Young Ki Choi received the B.S and M.S degrees in Mechanical engineering from Seoul National University in 1978 and 1980, respectively and the Ph.D. de-gree in mechanical engineering from the University of California at

Berkeley in 1986. He is currently a professor at the School of Mechanical Engineering, Chung Ang University, Korea. His research interests are in the area of micro/nanoscale energy conversion and transport, computational fluid dynamics, and molecular dynamics simulations.



Joon Sik Lee received the B.S and M.S degrees in Mechanical engineering from Seoul National University in 1976 and 1980, respectively and the Ph.D. degree in mechanical engineering from the University of California at Berkeley in 1985.

He is currently a professor at the School of Mechanical & Aerospace Engineering, Seoul National University, Korea. He is also the director of Micro Thermal System Research Center. His research interests are in the area of micro/nanoscale energy conversion and transport, thermal management for power generation and energy efficiency, and various convective heat transport phenomena such as pool boiling and nanofluid.